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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,756	04/14/2005	Martin Raubuch	SC12303EM	2224

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EXAMINER	
PARTRIDGE, WILLIAM B	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/531,756	RAUBUCH, MARTIN	
	Examiner	Art Unit	
	William B. Partridge	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10, 14-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 14-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the preliminary amendment filed on April 14, 2005.

2. Claims 3, 4, and 7-10 have been amended.

3. Claims 11-13 have been canceled.

4. Claims 14-21 have been added.

5. Claims 1-10 and 14-21 are pending and have been examined.

Information Disclosure Statement

6. The information disclosure statement (IDS) submitted on April 14, 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

7. The disclosure is objected to because of the following informalities:

On page 2, line 13 "a first aspect" should be "a second aspect".

The arrangement of the specification is not in the preferred layout.

Appropriate correction is required.

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in

upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Objections

8. Claims 1, 2, and 5 are objected to because of the following informalities:

As per claim 1, line 6 should conclude with "block; and"

As per claim 2, line 7 should conclude with "block; and"

As per claim 5, line 5 should conclude with "characteristics; and".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-7, 9, 14, 15, 17 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by **Scales, III et al.** (US 5,996,057 A).

Claim 1

"An arrangement for vector permutation in a single-instruction multiple-data microprocessor, the arrangement comprising:

a permutation logic block coupled to receive and permutate vectors from at least one vector register according to control parameters;" **Scales** discloses performing a Permute-With-Replication operation on input vectors loaded into vector registers (Column 2 lines 59-66, Fig 2).

"a plurality of control registers, each coupled to selectively provide control parameters to the permutation logic block; and," **Scales** discloses using control vectors located in control registers to control the Permute-With-Replication operation (Column 2 line 59 – Column 3 line 13, Fig 2).

"control means coupled between the plurality of control registers and the permutation logic block and arranged for selecting one of the plurality of control registers and for providing the control parameters from the selected one of the plurality

of control registers to the permutation logic block." **Scales** discloses selecting a control vector and where the Permute-With-Replication operation is performed on the input vectors as specified by the control vector (Column 2 line 59 – Column 3 line 13, Fig 2).

Claim 2

"A single-instruction multiple-data microprocessor vector permutation system comprising:

at least one vector register;" **Scales** discloses the use of a vector register (Column 2 line 59 – Column 3 line 13, Fig 2).

"a permutation logic block coupled to receive and permutate vectors from the at least one vector register according to control parameters;" **Scales** discloses performing a Permute-With-Replication operation on input vectors loaded into vector registers (Column 2 lines 59-66, Fig 2).

"a plurality of control registers, each coupled to selectively provide control parameters to the permutation logic block; and," **Scales** discloses using control vectors located in control registers to control the Permute-With-Replication operation (Column 2 line 59 – Column 3 line 13, Fig 2).

"control means coupled between the plurality of control registers and the permutation logic block and arranged for selecting one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block." **Scales** discloses selecting a control

vector and where the Permute-With-Replication operation is performed on the input vectors as specified by the control vector (Column 2 line 59 – Column 3 line 13, Fig 2).

Claim 3

"The arrangement of claim 1 further comprising a negate block coupled to the control means and coupled to receive and selectively negate vectors from the permutation logic block according to the control parameters received from the control means, wherein the control parameters include permutation parameters and negate parameters." **Scales** discloses all the limitations of claim 1 and performing a vector operation on the output vector in the output register (Column 8 lines 32-33, Fig 6). A vector negation is a specific type of vector operation. The control parameters both create the control vector for the Permute-With-Replication operation and perform vector operations on the output vector (Fig 6).

Claim 4

"The arrangement of claim 1 wherein the control means includes at least one counter arranged to provide a sequential order for selecting one of the plurality of control registers." **Scales** discloses all the limitations of claim 1 and a serially dependent chain of binary functions to be performed within the vector registers (Column 3 lines 11-13). Serially dependent functions require for operations to be performed sequentially. It is inherent that in order for progression of sequential order a counter of some kind must be present.

Claim 5

"A method for vector permutation in a single-instruction multiple-data microprocessor, the method comprising the steps of:

providing vectors to be permutated;" **Scales** discloses loading vectors into vector registers for a Permute-With-Replication operation (Column 2 lines 59-66, Fig 2).

"selecting one of a plurality of control registers, each control register containing parameters for determining permutation characteristics;" **Scales** discloses the operational code or result of a previous computation selecting the control vector (Column 3 lines 3-5). A control register contains the control vector; therefore by selecting the control vector the containing register is also selected.

"permutating the vectors according to the parameters of the selected control register." **Scales** discloses a Permute-With-Replication operation performed on input vectors as specified by the control vector (Column 2 lines 59-66). The control vector is contained in a control register.

Claim 6

"The method of claim 5 wherein the control register parameters are also used for determining negate characteristics and the step of permutating further includes the step of selectively negating the vectors according to the parameters of the selected control register." **Scales** discloses all the limitations of claim 5 and performing a vector operation on the output vector in the output register (Column 8 lines 32-33, Fig 6). A

vector negation is a specific type of vector operation. The control parameters both create the control vector for the Permute-With-Replication operation and perform vector operations on the output vector (Fig 6).

Claim 7

"The method of claim 5 wherein the step of selecting further includes the following of a sequential order of the plurality of control registers." **Scales** discloses all the limitations of claim 5 and a serially dependent chain of binary functions to be performed within the vector registers (Column 3 lines 11-13). Serially dependent functions require for operations to be performed sequentially.

Claim 9

"The arrangement of claim 4, wherein the sequential order includes automatic sequencing through a set of programmable control parameters." **Scales** discloses all the limitations of claim 4 and that the control vector can be specified in the operational code or the result of a computation previously performed (Column 3 lines 3-5). Automatic sequencing is inherent in that the control vector can be the result of a computation previously performed.

Claim 14

In view of the rejection made to claim 3, which contains the same limitations, claim 14 is rejected as well.

Claim 15

In view of the rejection made to claim 4, which contains the same limitations, claim 15 is rejected as well.

Claim 17

In view of the rejection made to claim 9, which contains the same limitations, claim 17 is rejected as well.

Claim 20

In view of the rejection made to claim 9, which contains the same limitations, claim 20 is rejected as well.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 8, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Scales, III et al.** (US 5,996,057 A) in view of **Wang** (US 6,886,124 B2).

Claim 8

"The arrangement of claim 4, wherein the sequential order includes automatic sequencing through a set of fixed control parameters." **Scales** discloses all the limitations of claim 4 and automatic sequencing (Column 3 lines 3-5) but does not disclose the use of fixed control parameters. However, **Wang**, in an analogous art, discloses loading fixed values for use in a configuration sequence (Column 29 lines 57-59). Automatic sequencing is inherent in that the control vector can be the result of a computation previously performed.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of **Wang** into the teaching of **Scales** to use fixed control parameters. The modification would have been obvious because one of ordinary skill in the art would have been motivated to have fixed values available to allow for faster access of commonly used parameters as opposed to having to program them over and over.

Claim 16

In view of the rejection made to claim 8, which contains the same limitations, claim 16 is rejected as well.

Claim 19

In view of the rejection made to claim 8, which contains the same limitations, claim 19 is rejected as well.

13. Claims 10, 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Scales, III et al.** (US 5,996,057 A) in view of **Curry** (US 4,935,891 A).

Claim 10

"The arrangement of claim 4, wherein the sequential order is cyclical." **Scales** discloses all the limitations of claim 4 but does not disclose a cyclical sequential order. However, **Curry**, in an analogous art, discloses the use of cyclical sequential order (Column 4 line 67 – Column 5 line 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of **Curry** into the teaching of **Scales** to have cyclical sequential order. The modification would have been obvious because one of ordinary skill in the art would have been motivated to be able to easily repeat the same order of operations and to be able to implement loop functions.

Claim 18

In view of the rejection made to claim 10, which contains the same limitations, claim 18 is rejected as well.

Claim 21

In view of the rejection made to claim 10, which contains the same limitations, claim 21 is rejected as well.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Argarwal et al. (US 5,758,176 A) teaches vector processing in a SIMD processor that includes a control unit to control vector operations.

Omoda et al. (US 4,825,361 A) teaches vector processing with a control circuit.

Bhandarkar et al. ("Vector Extensions to the VAX Architecture") teaches vector processing with control registers.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William B. Partridge whose telephone number is (571) 270-1402. The examiner can normally be reached on M-TR 7:30 - 5:00, alternate F 7:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chameli Das can be reached on (571) 272-3696. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Examiner: William B Partridge
Date: September 18, 2006

Chameli Das
CHAMELI DAS
SUPERVISORY PATENT EXAMINER
9/18/06